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Low-Voltage, Super-Junction Technology

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The scalability of super-junction and super-field power MOSFET technologies to breakdown voltages lower than 250 V is investigated. The influence of device geometry and process architecture on the switching figures of merit of these relatively new classes of power switches with a breakdown voltage rating of 80 V is presented. The current flow and field distributions inside these devices are described. Using Gauss's law, the field-induced compensation of the doping density in the drift region during the blocking state of both super-junction and super-field MOSFETs is calculated from the knowledge of the lateral field distributions. It is shown that the problem associated with imperfect charge compensation at the edge of the die for a super-field-effect power MOSFET structure can be avoided by using an unconventional racetrack layout design.

Keywords: Power, MOSFET, Super, Junction, Field, Modulation, Edge Termination, Racetrack

1 - Introduction

High-voltage power MOSFET technologies based on the super-junction concept have attracted a great deal of attention over the past decade, although the super-junction concept was proposed a quarter century ago [1]. High-voltage, super-junction MOSFETs are now available commercially [2]. The specific on-resistance of this new class of power MOSFETs at a breakdown voltage rating of 600 V is lower than that of conventional power MOSFETs by a factor of three or more, and is below that of the silicon limit [3].

Although the super-junction concept is applicable at any voltage, its application to low-voltage ranges (below 250 V) has lagged behind [4]. The resistance of the drift layer of power MOSFETs is more than 80 % of their total on-resistance at breakdown voltages of 80 V and higher. Therefore, reduction of the drift layer resistance by adopting the super-junction concept is desirable. This is especially true in fast-switching applications, because with reduction in on-resistance, there is no concomitant increase in gate-related capacitances. Power switching devices designed using the super-junction technology will have better switching figures of merit than those designed using high-cell-density, conventional power MOSFET technology.

MOS barrier-based, super-junction MOSFETs [5] employ deep-trench capacitors and avoid the need for multiple epitaxy processes, which are needed to realize buried vertical alternate P-N junctions associated with the junction-based, super-junction technology. The conventional trench technology can also be easily adapted to fabricate vertical MOS barrier-based, super-junction MOSFETs that belong to the same class as the vertical charge-control MOSFETs [6].

In this paper, we begin with a brief review of the avalanche breakdown behavior of the drift regions associated with conventional and super-junction MOSFETs from a field theoretic point of view. We use Gauss's law to show how the existence of an electric field lateral to current flow (the direction of applied drain-to-source voltage) can reduce the effectiveness of the ionized impurities during the blocking state of the device. Because of this field-modulation effect, the specific on-resistance of a super-junction drift region can be lower than that of a conventional drift layer for a given breakdown voltage. The lateral electric field

can be generated in the drift region either by incorporating PN junctions or MOS capacitors with appropriate electrical connections. We use the name super-field-effect transistors (SFETs) to distinguish the MOS barrier-based, super-junction transistors from the junction-based, super-junction MOSFET transistors (SJFETs).

We then study the scalability of SJFETs and SFETs to low-voltage ranges (60 V – 250 V), using analytical and numerical methods, respectively. We then compare the device behavior and switching performance of somewhat optimized and structurally different SJFETs and SFETs designed for a breakdown voltage of 80 V. It is shown using the lateral field distributions in the drift and body regions of the devices studied in this paper that the field-modulation effect electrically lowers the drift region doping level by a factor of 10 during the blocking state of the device. This improves the performance of the super-junction devices compared to conventional power MOSFETs.

The figures of merit of four structurally different SJFETs and SFETs, and a conventional state-of-the-art TrenchFET with a breakdown voltage rating of 80 V, are compared with each other. The edge termination problem associated with the SFET power device structure is addressed briefly, and it is shown that by utilizing a racetrack layout with a proper choice of radius of curvature at the turning points, breakdown voltages can be achieved that are close to ideal. It is shown that for SFETs fabricated under identical processing conditions, the breakdown voltage of the racetrack design is about 15 % higher than that of the striped-cell design.

2 - Review of the Super-Junction Concept

The drift regions of a double-diffused power MOSFET (DMOSFET) and a SJFET are shown in Figure 1 and Figure 2, respectively. In the DMOSFET structure, when the drain is reverse biased, the depletion region between the body and the drift region punches through laterally from both sides and then spreads towards the drain in a substantially one-dimensional manner similar to a plane-parallel junction.

In the SJFET structure, the JFET region, comprised of body, drain, and body region, extends deep into the drain section. When the drain voltage is applied, the entire JFET region is first pinched off laterally, establishing a lateral electric field. Further increase in drain potential increases the vertical electric field until the device breaks down due to impact ionization. In both n-channel DMOSFETs and SJFETs, the electric field in the drift and body regions of these device structures satisfies Gauss's law:

$$\nabla.\vec{E} = \frac{q(N_D - N_A + n - p)}{\varepsilon_s} \qquad (1),$$

where $\vec{E}$ is the electric field, q is the magnitude of charge of an electron, ε_s is the dielectric permittivity of silicon, and N_D and N_A are the ionized donor and acceptor densities of the drift and body regions, respectively. *n* and *p* denote electron and hole densities, which we will ignore in depleted sections for simplicity.

The electric field in the drift region of the DMOSFET structure, shown schematically in Figure 1, varies substantially along the drain-to-source direction. Equation 1 then becomes a one-dimensional, first-order differential equation, and its solution can be easily shown to be

$$\vec{E}(z) = \hat{z}\frac{qN_D}{\varepsilon_s}(W - z) \qquad (2),$$

where W is the thickness of the drift region, and the boundary condition used is that the electric field is zero at $z = W$ (at the end of the drift region). The electric field peaks at the junction. The potential can be calculated by integrating the electric field given in Equation 2 to be

$$V(z) = \frac{qN_D}{\varepsilon_s}(Wz - \frac{z^2}{2}) \qquad (3).$$

The avalanche breakdown voltage, BV, for the DMOSFET structure can be calculated [7] analytically by using the electric field given in Equation 2 in the ionization integral, and equating that to 1, such as

$$A\int_0^W E^7(z)dz = 1 \qquad (4),$$

where A is the ionization coefficient in silicon.

The integral in Equation 4 can be easily calculated, and one finds that the critical depletion region, W_c, at the point of avalanche breakdown is related to the doping density as

$$W_c = \left(\frac{8}{A}\right)^{\frac{1}{8}}\left(\frac{\varepsilon_s}{qN_D}\right)^{\frac{7}{8}} \qquad (5).$$

Once the critical depletion layer width is known, the avalanche breakdown voltage can be calculated from Equation 3 to be

$$BV = \frac{1}{2}\left(\frac{8}{A}\right)^{\frac{1}{4}}\left(\frac{\varepsilon_s}{qN_D}\right)^{\frac{3}{4}} \qquad (6).$$

The specific on-resistance of the drift region of the DMOSFET transistor can be easily calculated using Equation 5 as

$$R^c_{drift} = \frac{W_c}{q\mu_n N_D} = \left(\frac{8\varepsilon_s^7}{A}\right)^{\frac{1}{8}}\frac{1}{\mu_n}\frac{1}{(qN_D)^{\frac{15}{8}}} \qquad (7).$$

On eliminating the doping density of the drift layer between Equations 6 and 7, we get the following celebrated equation that relates specific on-resistance of the drift layer to its avalanche breakdown voltage:

$$R^c_{drift} = \frac{2A^{\frac{1}{2}}}{\mu_n\varepsilon_s}BV^{2.5} \qquad (8).$$

Equation 8 shows that the specific on-resistance of the drift layer is proportional to the avalanche breakdown voltage raised to the power of 2.5. It is considered to be the silicon limit. It is important to realize that this result assumes a one-dimensional description of the drift region in the sense that there is no electric field in a direction transverse to the applied voltage.

The field distribution in the drift region (defined as the section depleted at reverse bias, and in the case of SJFET, consists of the body, drain, and body regions) of a SJFET structure is two dimensional because of the presence of vertical PN junctions (see Figure 2). The breakdown voltage of the SJFET structure can be obtained as before by requiring that the

ionisation integral at avalanche breakdown is equal to 1. For the SJFET geometry, we write Gauss's law as shown below.

In the fully depleted drain region

$$\frac{dE_z}{dz} + \frac{dE_x}{dx} = \frac{qN_D}{\varepsilon_s} \qquad (9),$$

where $E_x \; and \; E_z$ are the electric field components in the lateral direction, $\hat{x}$, and in the vertical direction, $\hat{z}$, respectively.

In the fully depleted body region

$$\frac{dE_z}{dz} + \frac{dE_x}{dx} = -\frac{qN_A}{\varepsilon_s} \qquad (10),$$

where N_A is the ionized acceptor density.

In general, the field equations (Equations 9 and 10) have to be solved subject to appropriate boundary conditions. Here we propose in an adhoc manner that in the drain region ($0 \le x \le x_n$) the lateral electric field satisfies the equation

$$\frac{dE_x}{dx} = \frac{qN_D}{\varepsilon_s} \qquad (11),$$

and in the body region ($-x_p \le x \le 0$) the lateral electric field satisfies the equation

$$\frac{dE_x}{dx} = -\frac{qN_A}{\varepsilon_s} \qquad (12),$$

where x_n and x_p are the width of the N drain and P body regions, respectively.

Using Equations 11 and 12 in Equations 9 and 10, we obtain for the entire drift region (both the depleted drain and body regions) the following equation for E_z :

$$\frac{dE_z}{dz} = 0. \qquad (13).$$

The continuity of the x component of the electric field at the lateral PN junction implies that

$$x_n N_D = x_p N_A \qquad (14).$$

Equation 13 is the charge neutrality condition expected for PN junctions. The lateral field peaks at the junction and the vector electric field in the quasi two-dimensional approximation can be written in the drain region ($0 \le x \le x_n$) as

$$\vec{E}(x,z) = \hat{z}\frac{V_D}{W} + \hat{x}\frac{2qN_D}{\varepsilon_s}(x - \frac{x_n}{2}) \qquad (15),$$

and in the body region ($-x_p \le x \le 0$) as

$$\vec{E}(x,z) = \hat{z}\frac{V_D}{W} - \hat{x}\frac{2qN_A}{\varepsilon_s}(x + \frac{x_p}{2}) \qquad (16).$$

Following Huang, Amartunga, and Udrea [8], we assume that the horizontal field can be neglected near avalanche breakdown compared to the vertical field, and assume that the path of the ionization integral can be taken along the drain-to-source direction. Using Equation 15 in Equation 4, and carrying out the trivial integration, we find that the critical depletion width, W_c, is related to breakdown voltage as

$$W_c = A^{\frac{1}{6}} BV^{\frac{7}{6}} \qquad (17).$$

Upon taking a dot product of both sides of Equation 16 by the unit vector, $\hat{x}$, we get

$$N_D = \frac{\varepsilon_s E_L^c}{q x_n} \qquad (18),$$

where E_L^c is the peak lateral field at $x = 0$ (at the vertical PN junction). E_L^c is a parameter that cannot be obtained using a quasi two-dimensional analysis, but as we have mentioned earlier, it is assumed to be smaller than the vertical critical field, $E_V^c \equiv \frac{BV}{W_c}$, which can be shown using Equation 17 to be

$$E_V^c = A^{-\frac{1}{6}} BV^{-\frac{1}{6}} \qquad (19).$$

Equation 17 and 18 can be used to obtain the following relationship between the specific on-resistance and the avalanche breakdown voltage for the super-junction drift region:

$$R_{drift}^s = \frac{W_c}{q\mu_n N_D} = \frac{2A^{\frac{1}{6}} x_n BV^{\frac{7}{6}}}{\mu_n \varepsilon_s E_L^c} \qquad (20).$$

The specific on-resistance of the drift region of SJFET, according to this simple analysis, varies as the breakdown voltage to the 7/6 power rather than the 2.5 power for the conventional MOSFET. It must be pointed out, however, that we have in principle assumed that the peak lateral field is not a function of the breakdown voltage, which may not be correct. Different power law relationships between the specific on-resistance and the avalanche breakdown voltage for super-junction drift regions have been obtained by several authors employing different quasi two-dimensional approximations [9].

In order to obtain the unknown parameter in Equation 20, we compare the results of Equation 20 with that obtained by using MEDICI simulations for a super-junction drift region with a cell pitch equal to 5 microns [10]. The cell pitch is defined as twice the pitch of the vertical PN junctions. We find that a value of $E_L^c = 1.85x10^5$ V/cm is a good fitting parameter.

The specific on-resistance as a function of breakdown voltage, according to Equation 20, is plotted in Figure 3. It can be concluded that Equation 20 is in fair agreement with MEDICI calculations with a single fitting parameter. The specific on-resistance of the super-junction drift region as a function of two different cell pitches equaling 4 microns and 12 microns are shown in Figure 4 as a function of breakdown voltage. From Figure 4 it can be concluded that super-junction technology will have significant advantages at voltages higher than 500 V, and at smaller pitches of the unit cell. At a breakdown voltage of 250 V, super-junction devices with a 12-micron cell pitch will have 20 % lower on-resistance than conventional MOSFET devices. As the cell pitches become finer, super-junction devices becomes much better, but with the increased complexity of processing.

It is obvious, however, that the above analysis of the super-junction MOSFET is based on an adhoc assumption that the lateral electric field satisfies Equations 10 and 11, which may not be true in general. For a better understanding of the super-junction effect, we rewrite Equation 1 as shown below.
In the depleted drain region of SJFET

$$\frac{dE_z}{dz} = \frac{q}{\varepsilon_s} N_D^{Eff} \qquad (21),$$

where

$$N_D^{Eff} = (N_D - N_D^{Field}), \qquad (22),$$

and

$$N_D^{Field} \equiv \frac{\varepsilon_s}{q} \frac{dE_x}{dx} \qquad (23).$$

In the depleted body region of SJFET

$$\frac{dE_z}{dz} = -\frac{q}{\varepsilon_s} N_A^{Eff} \qquad (24),$$

where

$$N_A^{Eff} = (N_A - N_A^{Field}), \qquad (25),$$

and

$$N_A^{Field} \equiv \frac{\varepsilon_s}{q} \frac{dE_x}{dx} \qquad (26).$$

The above equations define the field-modulation effect in a quantitative manner. Depending upon the level of field-induced doping given by Equations 23 and 26, the level of the doping density of the ionized impurities will be effectively reduced. This makes the drain and body regions act like punch-through regions by reducing the slopes of the vertical electric fields in both the body and drain regions.

In the previous section we assumed that the field-induced doping densities exactly cancel the background ionized impurities. In general, the cancellation is not complete. It is possible, however, to render the drain and body regions of SJFET during the blocking state to act like virtual punch-through regions by proper design. Later we will determine the level of cancellation of the drift region doping due to the field-modulation effect for both SJFET and SFET structures.

The field modulation described above is different than the conductivity-modulation [11] effect during the on-state of the IGBT, where the injected electrons and holes modulate the conductance of the drift region to decrease the on-resistance. In the case of SJFET and SFET, the field modulation effectively lowers the doping density of the drift layer during the off-state of the device, leading to increased breakdown voltage. We will use the above equations later to estimate the level of field-modulation effect quantitatively in both the SJFET and SFET structures.

3.1 - Scalability of SJFET

Analytical, non-linear design equations that relate the breakdown voltage of the drift region of SJFET to the doping density, length, and width of the drift and body regions have been published recently by Strollo and Napoli [12]. By solving these non-linear, analytical equations, the specific on-resistance of SJFETs for different unit cell pitches can be obtained for different breakdown voltages. The results are shown in Figure 5. The results from our

quasi two-dimensional analysis are shown by the * symbol in Figure 5 for the sake of comparison. The discrepancy between the quasi two-dimensional analysis and analytical two-dimensional analysis becomes larger as the cell pitch reduces. A better fit can be obtained by using a different fitting parameter. The aspect ratio of SJFET as a function of breakdown voltage, as a function of unit cell pitch, is shown in Figure 6. The scaling behavior of the super-junction devices in the breakdown voltage range of 50 V to 250 V can be easily deduced from Figure 5 and Figure 6, especially for breakdown voltages higher than 80 V, where drift resistance is the dominant portion of the total on-resistance. For example, at 250 V, reducing the cell pitch from 3 um to 1 um will reduce the resistance by a factor of 2.5. However, this requires the aspect ratio of the P and N pillars to be increased from 8 to 23, respectively. While scaling super-junction devices, the cost and performance have to be taken into account and proper tradeoffs be carried out.

3.2 - Scalability of SFET Device Structure

A schematic two-dimensional cross-section of a power MOSFET whose drift region is interrupted by a MOS barrier rather than a PN junction, as in SJFET, is shown in Figure 7. In this device structure, the low-voltage portion of the power MOSFET can be viewed as connected to a deep-depletion trench capacitor. When the drain is reverse biased with respect to the body, the drift region is depleted from the body vertically and laterally from the buried source poly, which is connected to the source. The doping of the drift region of SFETs for a given breakdown voltage can now be increased because of the lateral field set up by the presence of the trench capacitor. The field-modulation effect described in the previous section for SJFETs will be operative in the SFET structure as well, and will lead to a lowering of the specific on-resistance for a given breakdown voltage compared to conventional MOSFETs.

The detailed device behavior and the role of the trench capacitor, and the resulting increase in the breakdown of this type of MOS device compared to the conventional power MOSFETs, has also been described by Temple [6]. It is interesting to note that in the SFET structure shown in Figure 8, there are two MOS gates: a turn-on and turn-off MOS gate, and a buried MOS gate that turns the device off by laterally pinching the drift region by deep depletion, which in turn establishes a horizontal electric field necessary to increase the breakdown voltage, as we discussed earlier.

The specific on-resistance of the SFET structures designed to support breakdown voltages from 60 V to 250 V have been derived using two-dimensional process and device simulators, and are shown in Figure 8. The thickness of the oxide in the trench capacitors present in the SFET structure must be such that it supports the rated voltage. A graph relating oxide thickness, doping density, and breakdown voltage for deep-depletion trench capacitors is given by Rusu and Bulucea [13].

The specific on-resistance of the SFET varies almost quadratically with the breakdown voltage. This may be related to the way key device parameters are used in the device simulation here, but we mention that similar conclusions have also been made in the literature [5]. This needs further study, but the behavior is to be expected from the field-modulation point of view, according to which the SFET behaves like a punch-through structure.

From Figure 8 it is clear that the on-resistance of the SFET is more than a factor of 2, lower than the current TrenchFET devices at breakdown voltages higher than 80 V. It must be noted that in Figure 8, we compare the total resistance of the device and not just the drift layer resistance. It is also important to note that etching deep trenches is not as complicated

a process compared to the process needed to generate alternately doped charge balance vertical pillars; however, growing thicker oxides can be challenging.

4 - On-State Behavior of SJFET and SFET

In this section we discuss the on-state device behavior of four different types of super-junction devices, all designed for a breakdown voltage rating of 80 V, using two-dimensional process and device simulations. The current flow lines inside two super-junction MOSFET structures used in this study are shown in Figure 9a and Figure 9b. The SJFET structure shown in Figure 9a employs a planar gate, and that shown in Figure 9b uses a trench gate. It is important to note that in the planar gate structure there are two JFET regions, one at the transition region between the channel and the drift, and the other in the extended JFET drift region. It is possible to optimize the JFET regions independently, but we have not done that here. The device structure shown in Figure 9b employs a trench gate and thus does not have the channel region JFET action. In designing these devices, we have used a 0.25-micron design rule for both the contact and the trench width. The device shown in Figure 9b is named as SJTFET to emphasize the trench gate.

The transition region between the N and P drift and body regions can be clearly seen in Figures 9a and 9b. The depletion-pinching effect can be seen constricting the electron flow during the on-state of the SJFET from the current flow lines in Figure 9a. The pinching action is seen at both the channel and the drift JFET regions. In the SJTFET structure, the JFET region at the channel is absent, which can be seen in Figure 9b.

The device structure shown in Figure 10a uses two trenches: one trench to house the control gate, and the other trench to house the polysilicon gate that is connected to the source. This device structure is named DTSFET; the first two letters in its name stand for dual trench. The device structure shown in Figure 10b uses a single trench to house both the gates, and is named STSFET; the first two letters in its name stand for single trench. The STSFET is more efficient in terms of silicon usage than the DTSFET, because unlike DTSFET, it uses the same space for both the gates. However, the processing of this structure is complex. In both these device structures, the deep polysilicon gate is connected to the source.

It can be concluded from the current flow lines in the DTSFET and STSFET (shown in Figure 10a and Figure 10b, respectively) that there is no depletion-pinching effect as in the SJFET structures. This is because in these structures there is no PN junction region in the drift section, and therefore, there is no intrinsic built-in potential due to diffusion and subsequent recombination of carriers from both sides of the junctions, as in the SJFET structures. Because of this, SFET structures will in principle have lower on-resistance than SJFET structures.

5 - Off-State Behavior and Field-Induced Doping in SJFET and DTSFET

We consider here the off-state behavior of SJFET and DTSFET. The doping profiles for these devices used for simulation are shown in Figures 11 and 12. The vertical components of the electric field distributions for these devices are shown in Figures 13 and 14. The vertical electric field components are relatively flat, indicating good punch-through type device design. With the doping level of $2X10^{16}\,cm^{-3}$ in the drift region, the vertical-field profile would have actually been steeper than that shown in Figures 13 and 14. The reduced slope of the vertical field is due to the presence of the lateral field in these structures in the drift and body regions, and the field-modulation effect described earlier.

The lateral-field distribution in the drift region of the SJFET and the DTSFET structures are shown in Figures 15 and 16, respectively. As we have discussed earlier, the slopes of these lateral fields are directly related to the degree of cancellation of the ionized impurities in the

drift regions. In the case of SJFET, the lateral field component shown in Figure 15 (the magnitude of the electric field is clipped at the transition region to show the slopes clearly) has two opposite slopes in the lateral direction necessary to compensate the oppositely ionized impurities (see Figure 11). The doping density, field-induced doping, and the effective doping density in the drift and body regions at mid-point across the SJFET device are shown in Figure 17. The effective doping density is the actual doping density reduced by the field-induced virtual doping density, as given by Equations 22 and 26. The effective doping density is of the order of $10^{15}\,cm^{-3}$, which is far larger than the value zero used in the one-dimensional analysis earlier. So the notion that the drift region in super-junction devices becomes intrinsic is not correct. What is correct, however, is that the drift region of a super-junction device behaves like a punch-through drift layer supporting higher breakdown voltages. The anisotropy of the effective doping density is due to anisotropy in the structure due to the MOS gate. This supports our field theoretical explanation of the impurity charge cancellation by the presence of the lateral field in the drift and body regions.

A similar analysis has been carried out for DTSFET, and the results are shown in Figure 18, where the doping density, field-induced virtual density, and the effective doping density in the middle of the DTSFET are shown. The effective doping density is again an order of magnitude lower than the background doping density. In this case, there are no N and P regions, so the argument often stated that the opposite ionized charges will effectively cancel each other, leading to an intrinsic region, is not tenable for DTSFET. The results shown in Figure 18 are in accordance with what has been stated earlier. It is important to note that it is possible that the lateral-field variation in poorly designed drift regions can in fact be such that there is an increase in the effective doping rather than a decrease, leading to reduced breakdown voltages. The results in this section clearly show that the drift regions of both the SJFET and DTSFET structures behave like virtual punch-through drift layers, despite being doped heavily.

6.1 - Edge Termination of SFET Device

We have so far described the core regions of the super-junction devices, whose drift regions have alternate layers of oppositely doped regions or deep-trench MOS capacitor structures. In practice, such layers have to be terminated. At the edges, three-dimensional effects will impact the avalanche breakdown characteristics of the device. A simple solution to address the edge-termination problem is to use a self-terminating racetrack layout. The selection of the curvature of the racetrack is important from the point of view of maximizing active area. A schematic drawing of the racetrack layout that has actually been implemented is shown in Figures 19 and 20, where various sections are as indicated. It is important to select the radius of curvature of the racetrack at the turning points. Our simulation shown in Figure 21 suggests for our design that a radius of curvature of about 15 μm will result in about 90 % of the ideal breakdown. It is also important to mention that in racetrack layouts the gates should be connected by proper design. Details including the fabrication methods of the racetrack design have been published recently [14].

The reverse breakdown characteristics of fabricated diodes from the same lot using the racetrack layout design and striped-cell design are shown in Figure 22. The reverse leakage current in both cases is in the range of a few nano Amperes per cm^2, and the breakdown voltage is sharp and close to the expected value. The breakdown voltage of the conventional stripe-type layout is found experimentally to be about 72 V, compared to 85 V for the racetrack design. The increase in the breakdown voltage for the racetrack design over the stripe design in this case is about 15 %, and is relatively immune from three-dimensional field distributions that occur at the edges of designs using a striped layout.

6.2 - Comparison of Figures of Merit

Finally, we address the performance characteristics of the low-voltage super-junction and super-field devices. The figure of merit for power semiconductor devices for load-switching applications is the specific on-resistance of the device. For switching applications such as PWM dc-to-dc converters, the figure of merit is the product of the specific on-resistance and the gate-drain charge, representing the plateau region in the gate-charge curve during which time the device switches on [15], [16]. We have calculated these figures of merit using two-dimensional process and device simulators for the different types of super MOSFETs studied in this paper. The results are shown in Figure 23, where we have also shown the Q_{gd} values. Although we have not designed these devices in the most optimal way, the performance trends of these devices are rather clear. The single-trench SFET has the best specific on-resistance, and the super-junction-trench MOSFET and SJTFET have the best switching performance. The Q_{gd} value of the SJTFET is significantly lower than others, because in this device the body region shares the gate charge more. The trench gate to a certain degree is shielded from the drain.

The switching figure of merit depends upon the cell density and device structure in a complex manner, and our results here should not be taken as definitive. It can be safely concluded, however, that at a breakdown voltage rating equal to 80 V, there exists a super MOSFET structure that outperforms the conventional power TrenchFET by a factor of two in its figures of merit.

7 - Conclusion

The scaling aspects of super-junction and super-field MOSFET device technologies for low voltages (below 250 V) have been described. The super-junction technology requires a significant amount of drift layer engineering. For super-junction MOSFETs, the challenge is to generate high-aspect-ratio, low-pitch vertical drift and body regions; and for super-field MOSFETs, the challenge is to integrate deep-trench MOS capacitors into the drift region. For both technologies, the challenge is also to integrate the complex drift regions with high-density MOS sections so that channel and other transition resistances do not become the limiting factors. Our analysis shows that the super-junction concept can be gainfully applied to voltages between 80 V and 250 V. The figures of merit of the super-junction and super-field power MOSFETs can be better by a factor of two or more over that of conventional power MOSFETs in that voltage range.

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[8] S.Huang, G.A.J.Amartunga and F.Udrea, "Analysis of SEB and SEGR in Super-Junction MOSFETs", IEEE Transactions on Nuclear Science, Vol. 47, p.2640, 2000

[9] Xing-Bi Chen etal , "Optimization of the Specific On-Resistance of the COOLMOS", IEEE Trans. On Electron Devices, 48, p.344,2001 and references there in. See also, T.Fujihira,"Theory of semiconductor super junction devices", Jpn. J. Appl. Phys., Vol.36,p.6254,1997, P.Shenoy etal, "Analysis of the effect of charge imbalance on the static and dynamic characteristic of super junction MOSFET", Proc. ISPSD, p.99,1999.

[10] We have used the MEDICI simulation results presented in ref.12 , Fig.9. We have used TCAD software, Suprem4 and MEDICI of Synopsis Corporation for two-dimensional process and device simulations presented in this paper

[11] For an account of conductivity modulation in IGBT, see for example, B.J. Baliga, Power Semiconductor Devices, PWS Publishing Company, Boston, 1996, Ch.8 p.426

[12] A.G.M. Strollo and E. Napoli, "Optimal On-Resistance versus Breakdown Voltage Tradeoff in Super junction Power Devices: A Novel Analytical Model", IEEE Transactions on Electron Devices, 48, p.2161, 2001
[13] For a discussion on deep depletion in trench capacitors see A. Rusu and C. Bulucea, "Deep Depletion breakdown voltage of SiO2/Si MOS capacitors", IEEE Trans. On Electron Devices ED-26, 201(1979). The simulation results presented in this paper can be used to determine optimal doping density and oxide thickness for a given breakdown voltage for designing SFET type devices.
[14] D.N. Pattanayak et al., "Super trench MOSFET including buried source electrode and method of fabricating the same," US Patent 7183610, 2007
[15] For an account of gate-drain charge in power MOSFET, see D.A.Grant and J.Gowar, " Power MOSFETs", Wiley, New York,1989, p.135
[16] Alex Huang, New Unipolar Switching Power Device Figures of Merit, Electron Device Letters, 25, 2004, p.298,

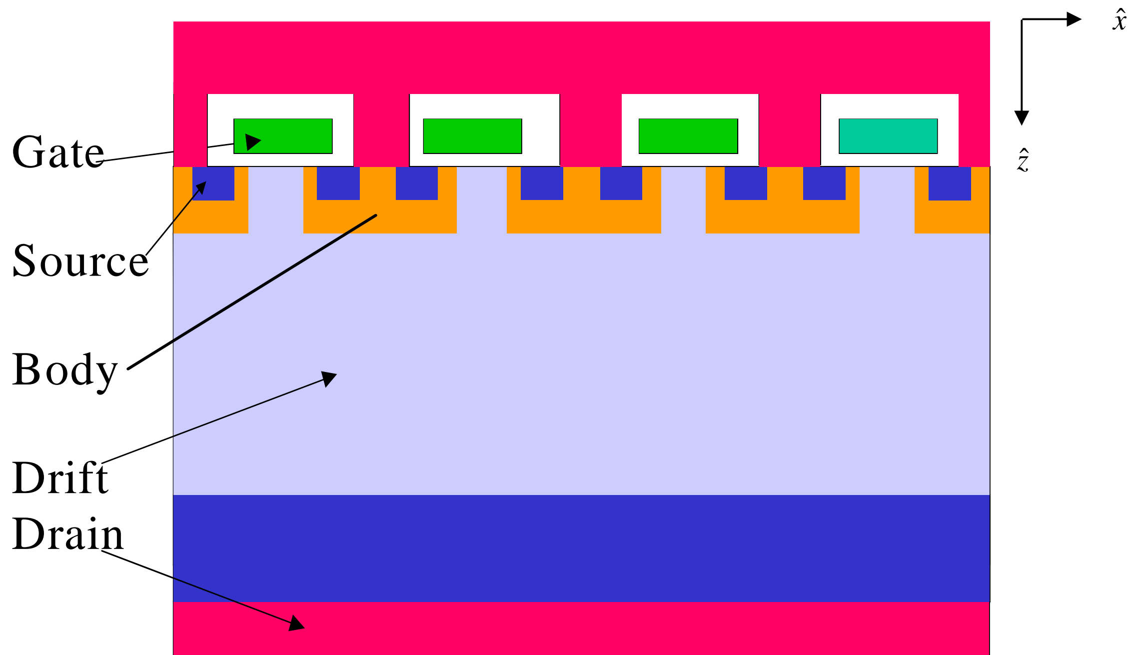

Figure 1 - Schematic Diagram of a Power MOSFET

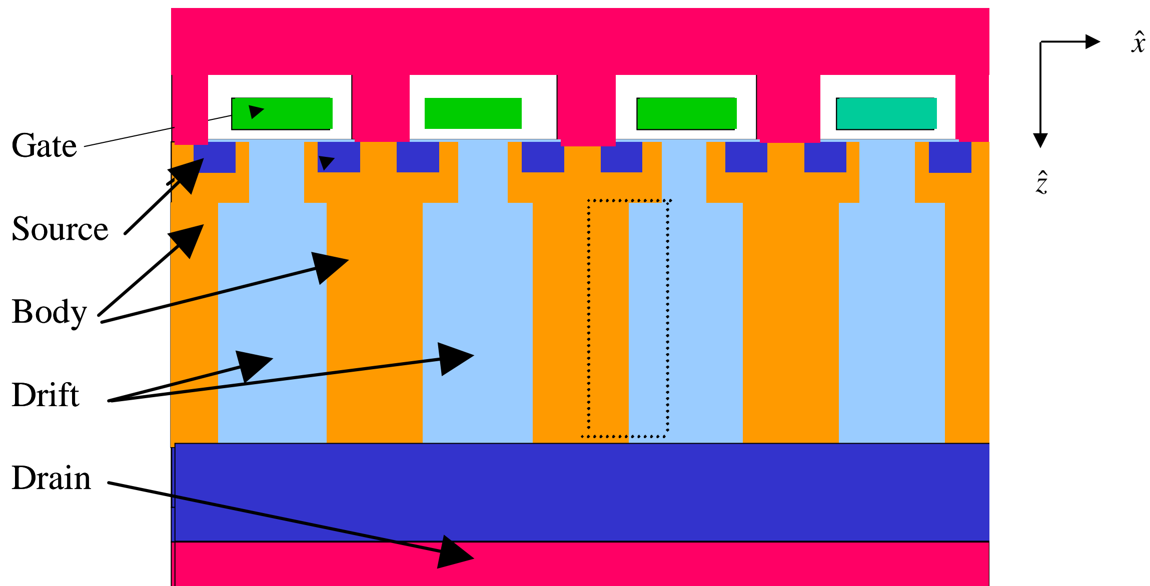

Figure 2 - Schematic Diagram of a Super-Junction Power MOSFET

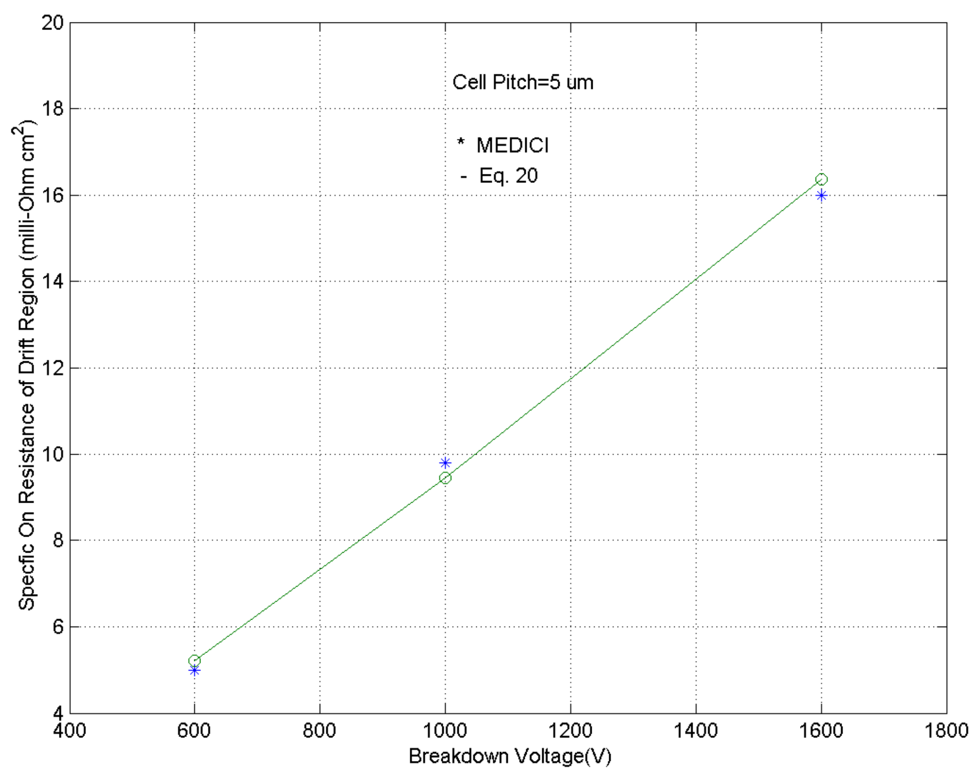

Figure 3 - Specific On-Resistance of SJFET From Equation 20 and MEDICI Simulation

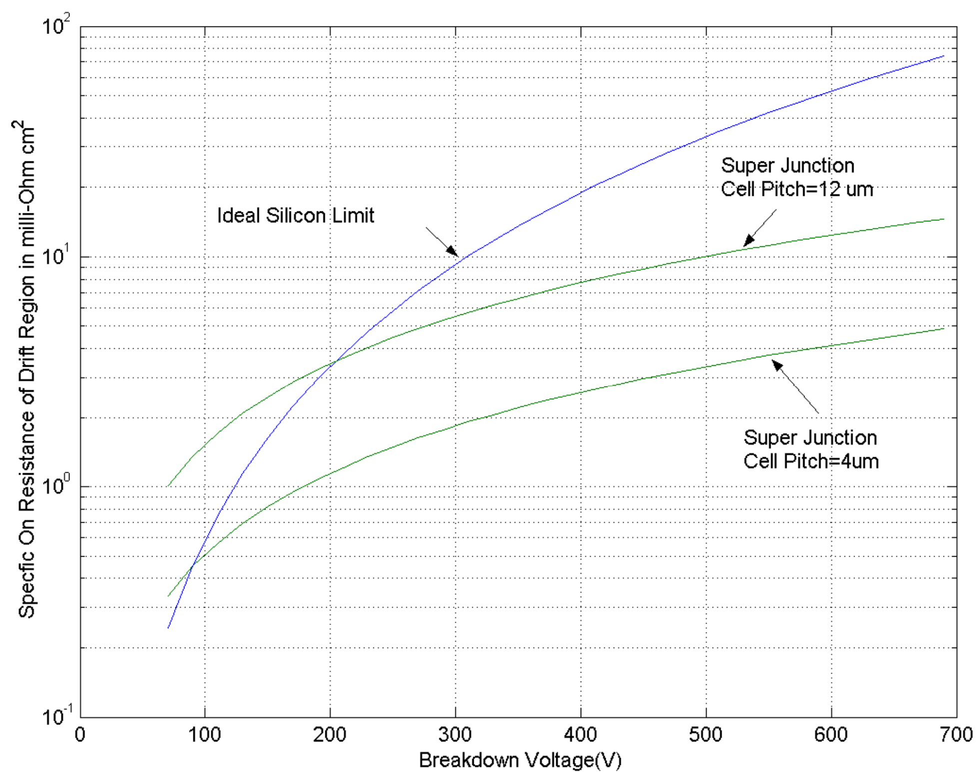

Figure 4 - Specific On-Resistance of Drift Region of Super-Junction vs Cell Pitch

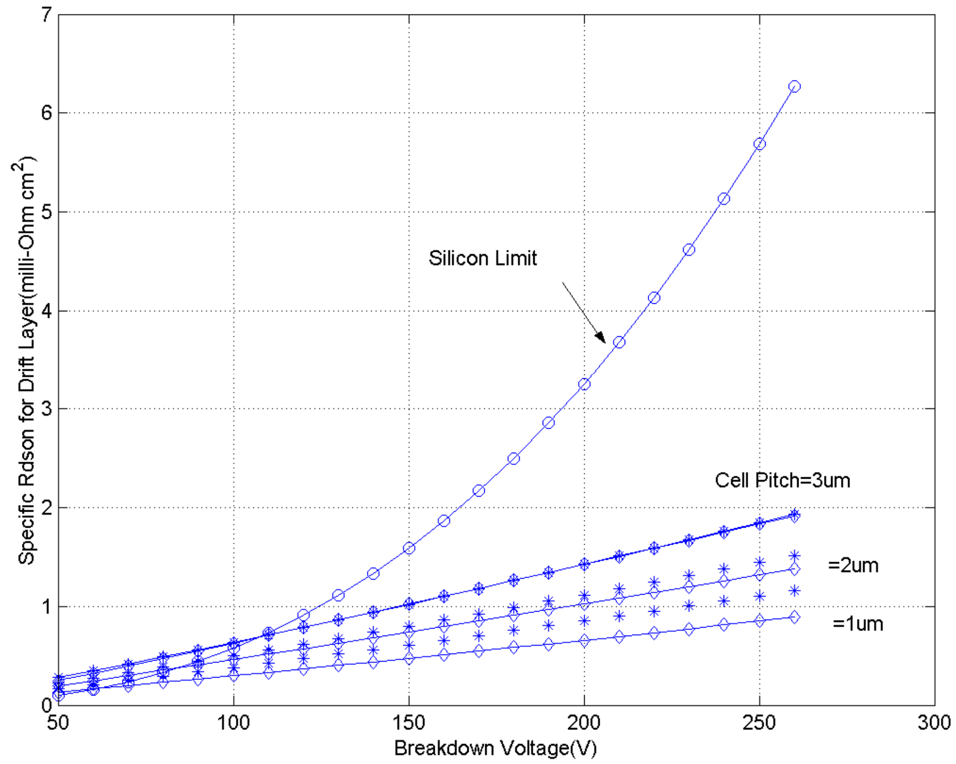

Figure 5 - Specific On-Resistance of Low-Voltage, Super-Junction Drift Regions vs. Cell Pitch

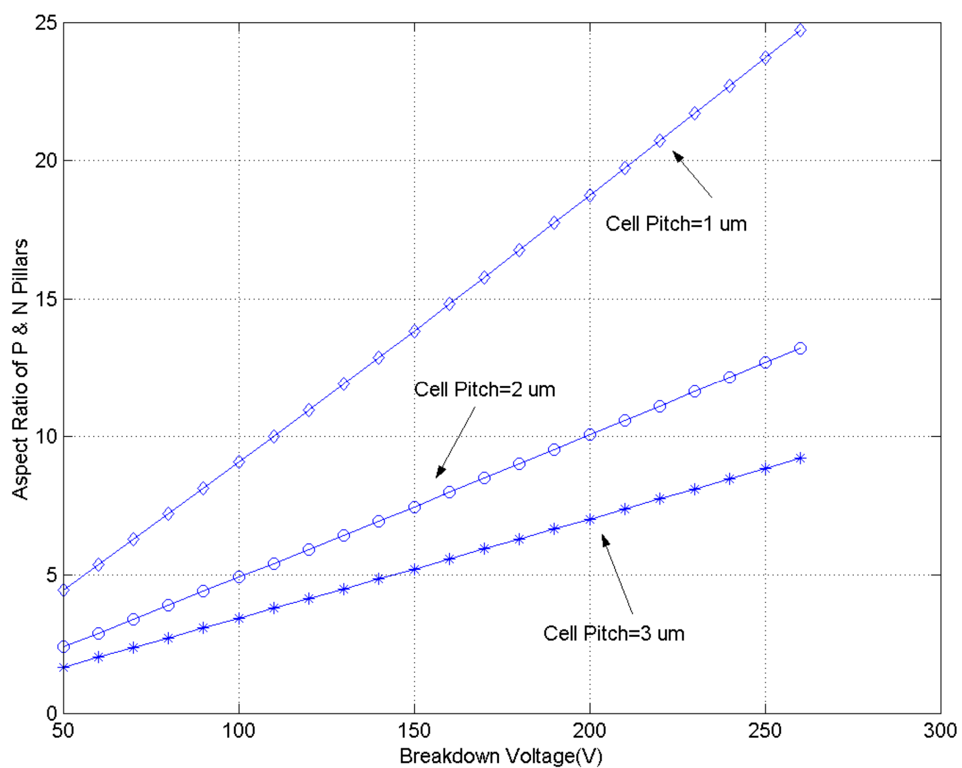

Figure 6 - Aspect Ratio of Vertical P & N Pillars as a Function of Cell Pitch and Breakdown Voltage

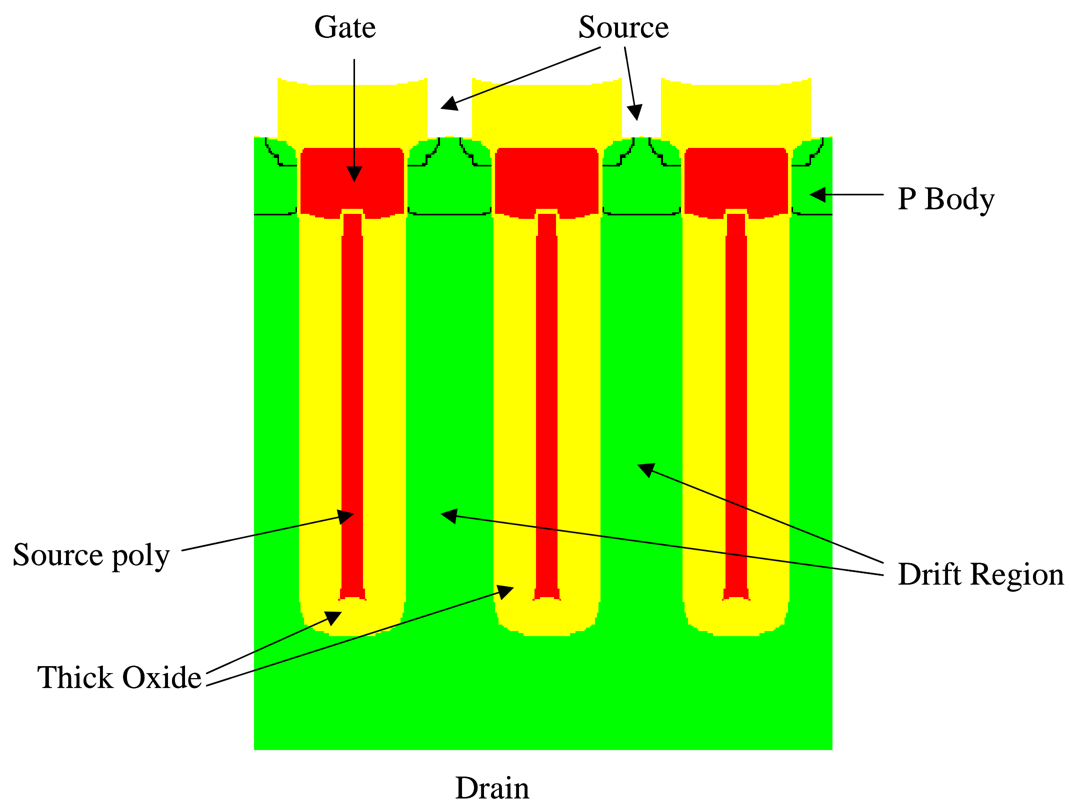

Figure 7 - Schematic Diagram of a SuperFET

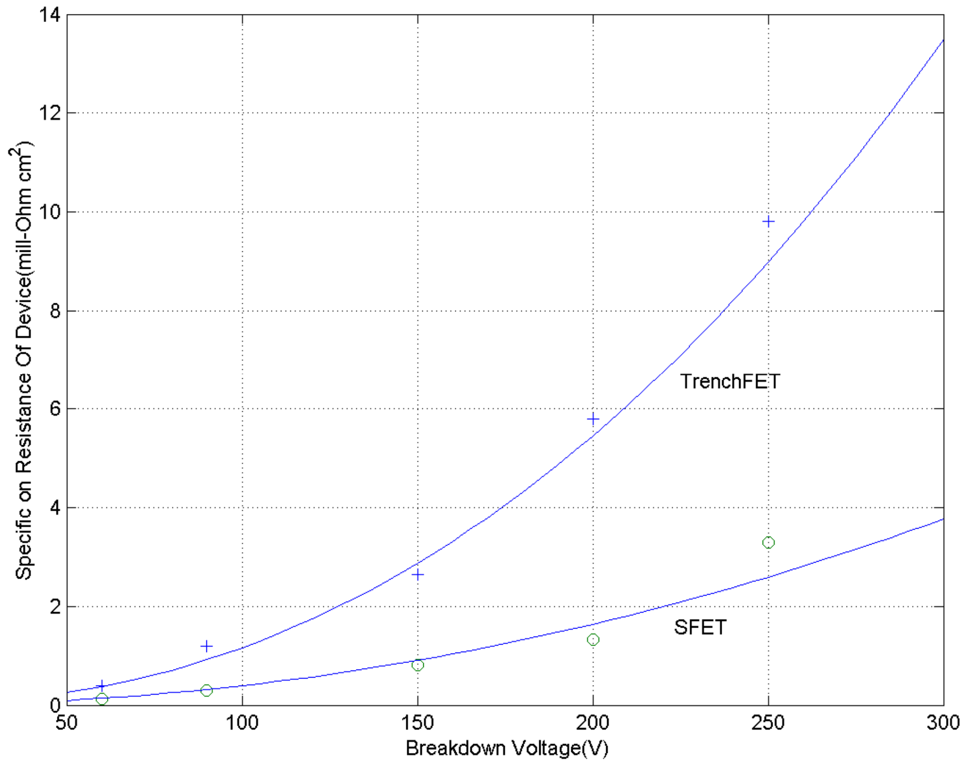

Figure 8 - Specific On-Resistance of SFET vs. Breakdown Voltage

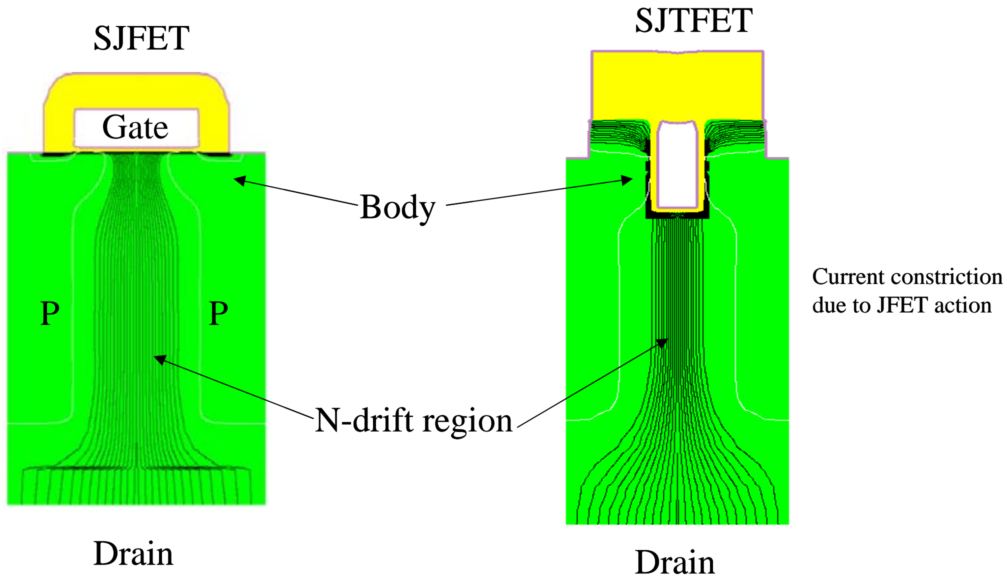

Figure 9a - Current Flow in SJFET

Figure 9b - Current Flow in SJTFET

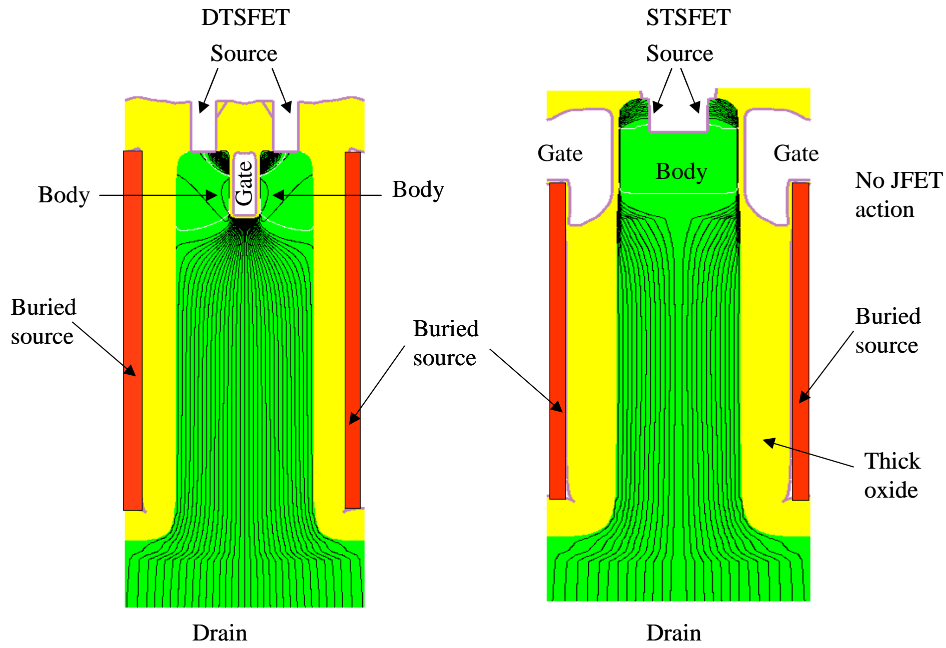

Figure 10a - Current Flow in DTSFET   Figure 10b - Current flow in STSFET

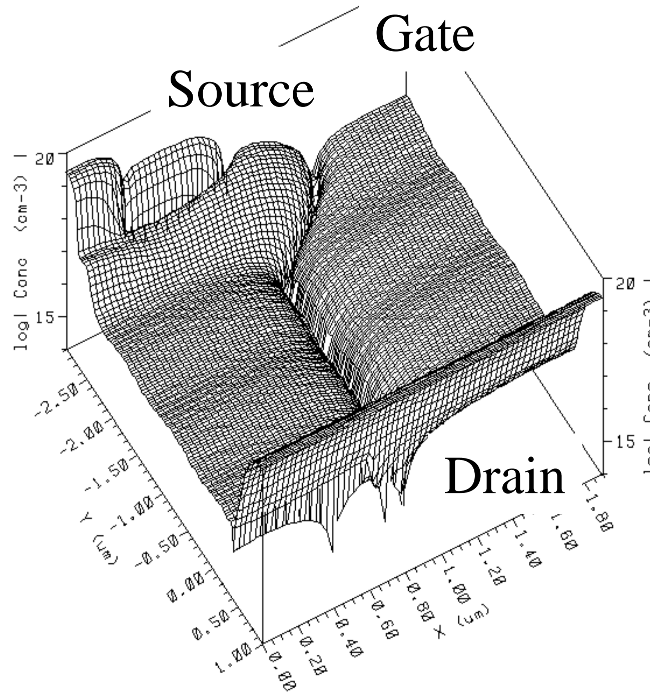

Figure 11 - Doping Profile of SJFET

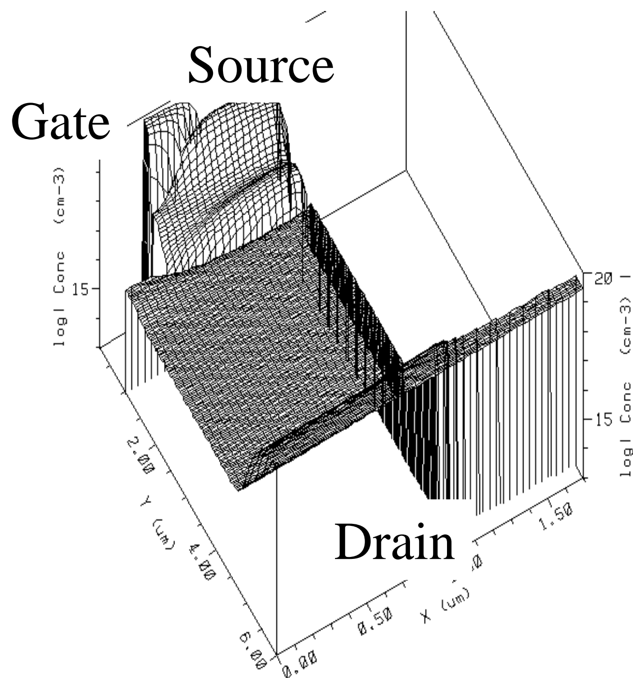

Figure 12 - Doping Profile of DTSFET

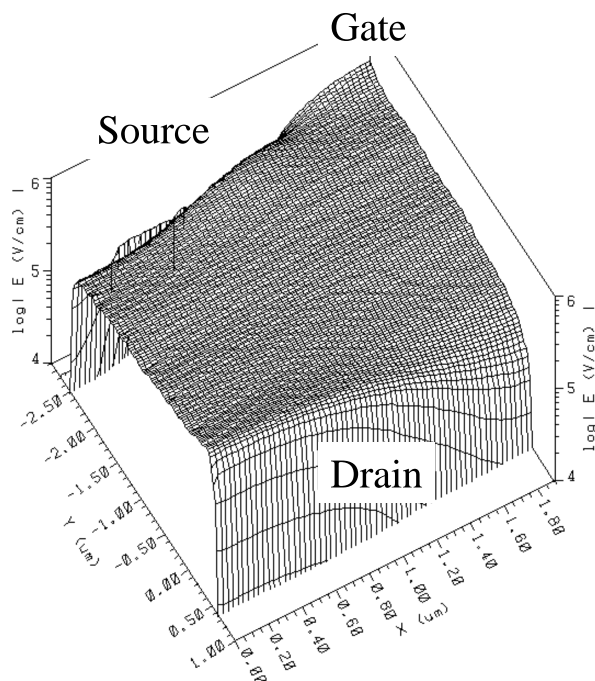

Figure 13 - Vertical Electric Field Component of SJFET

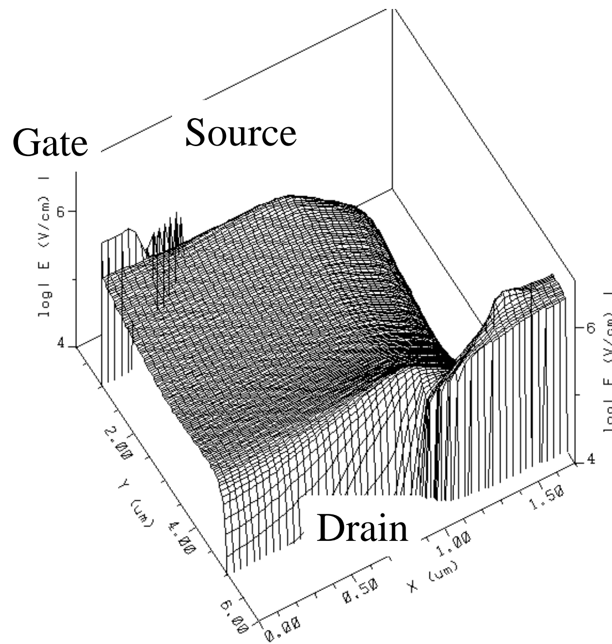

Figure 14 - Vertical Electric Field Component of DTSFET

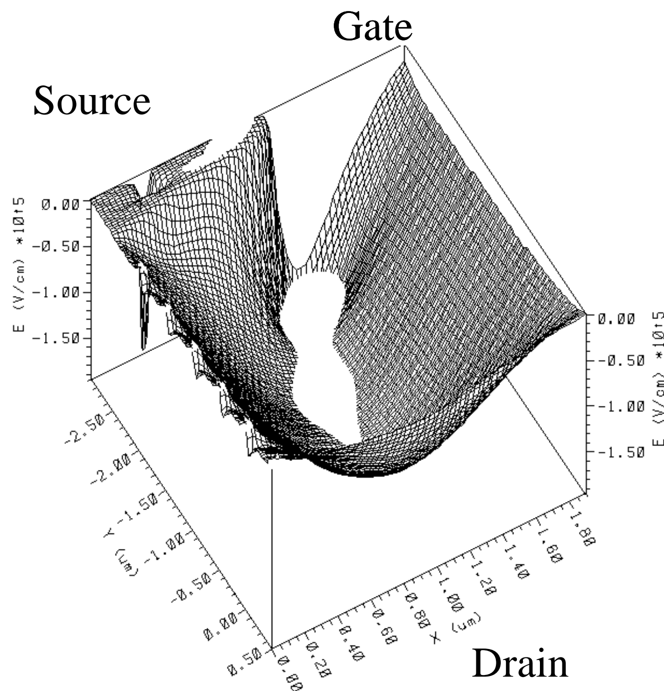

Figure 15 - Lateral Electric Field Component of SJFET

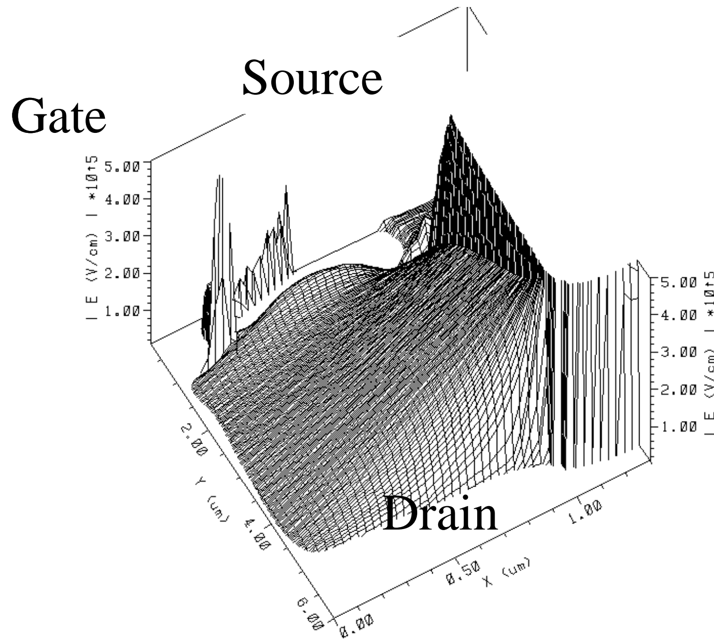

Figure 16 - Lateral Electric Field Component of DTSFET

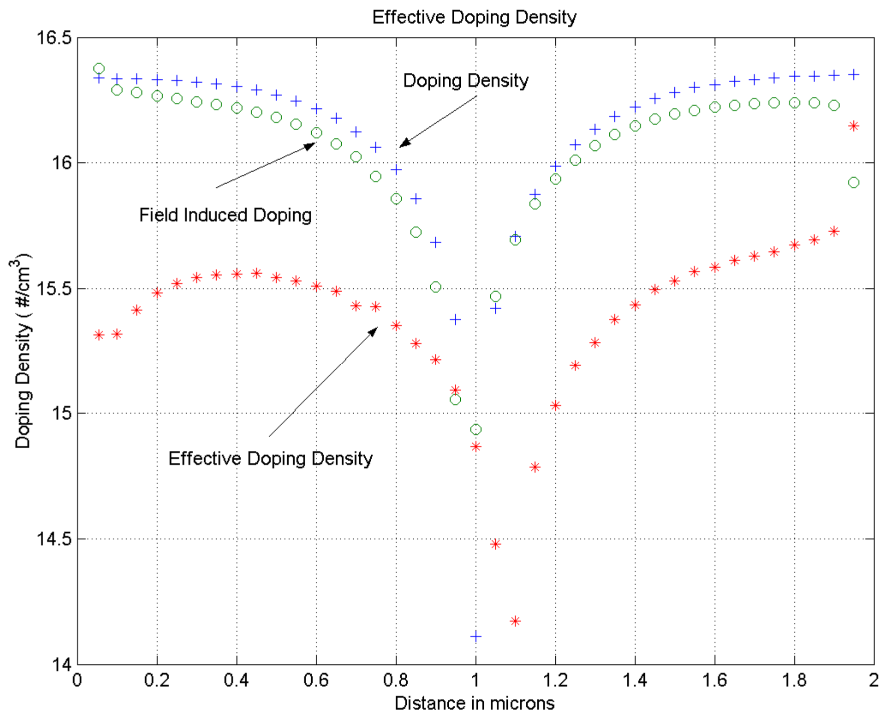

Figure 17 – Field-Modulation Effect in SJFET

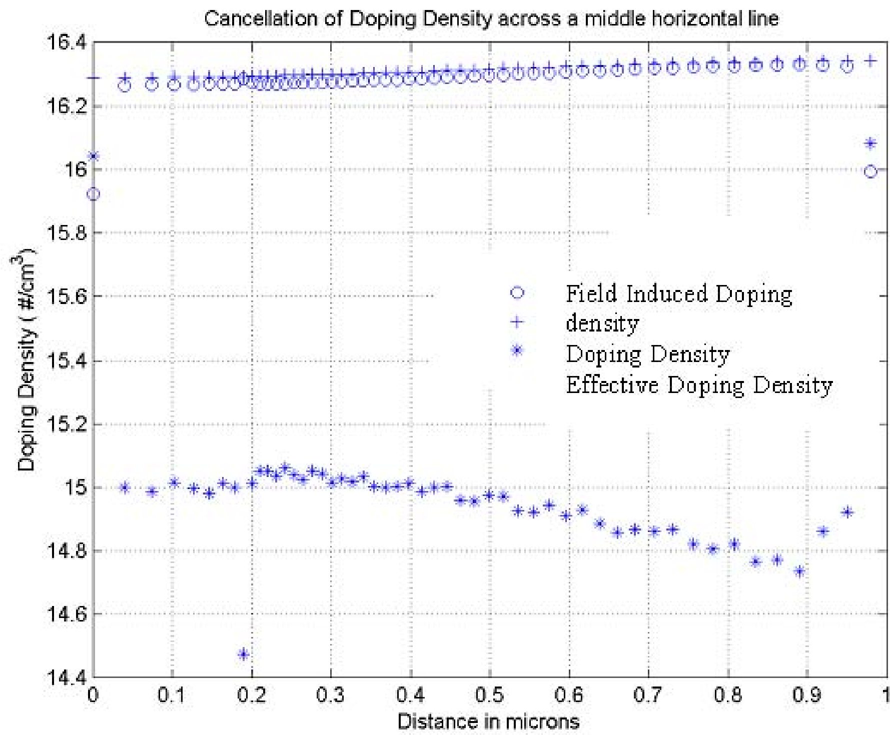

Figure 18 – Field-Modulation Effect in SFET

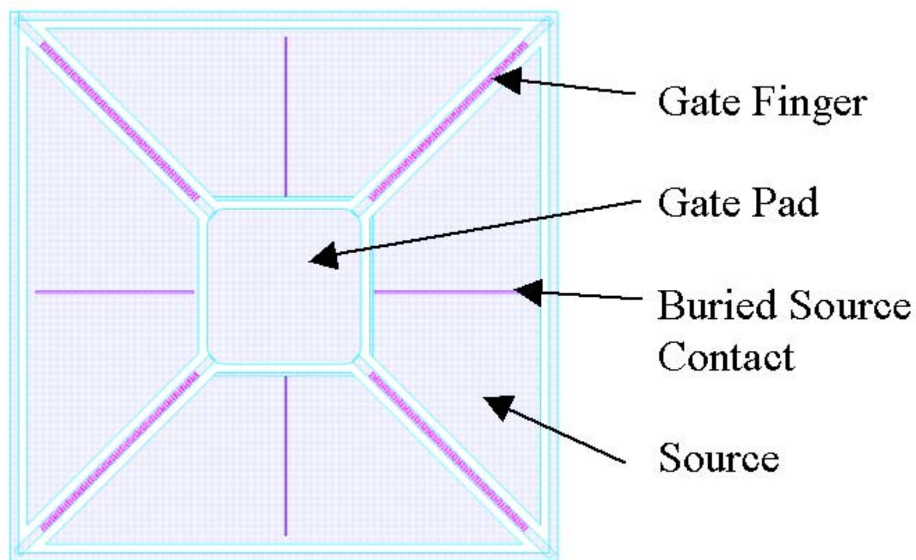

Figure19 - Racetrack Layout of SFET

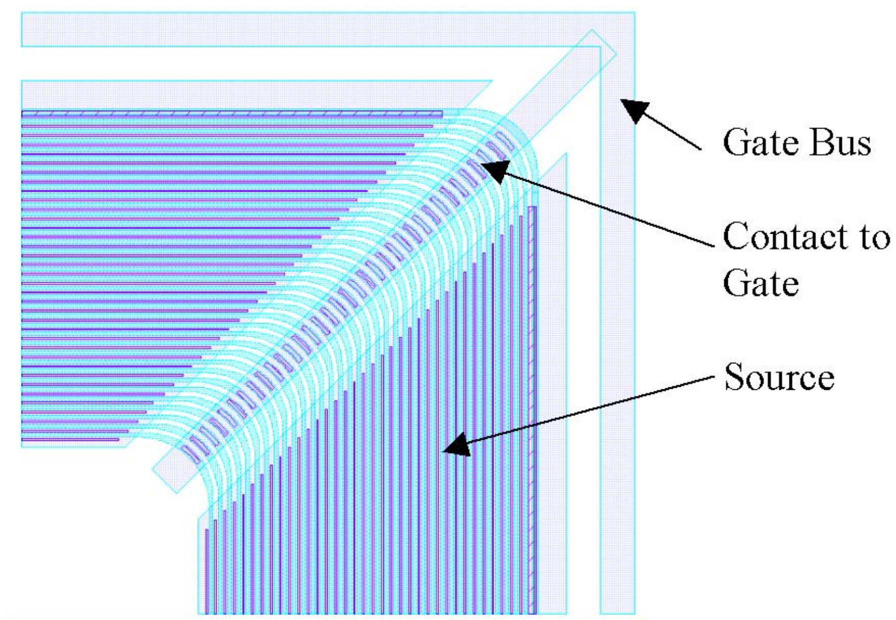

Figure 20 - Details of Racetrack Design

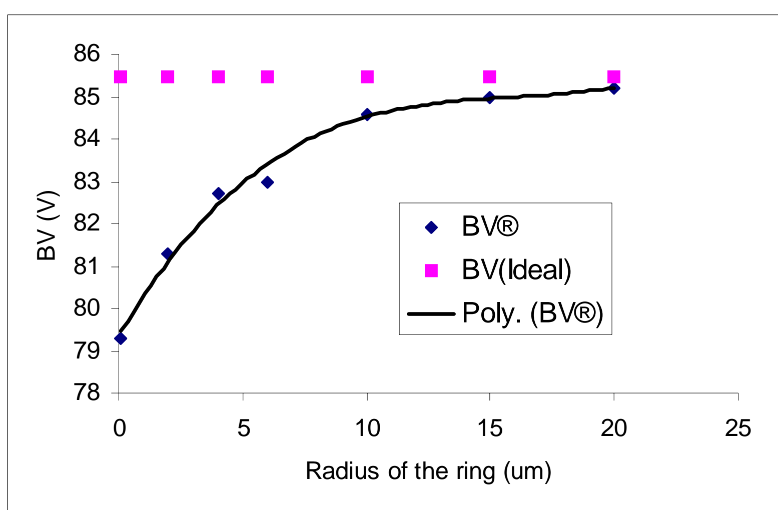

Figure 21 - Breakdown Voltage vs. Radius of Curvature of Racetrack

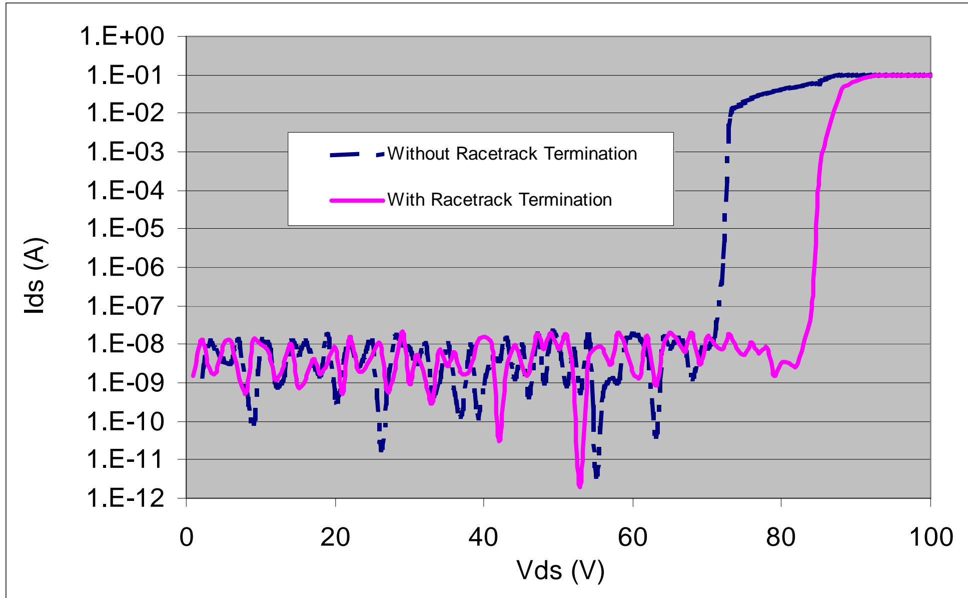

Figure 22 - Reverse Breakdown With and Without Racetrack Termination

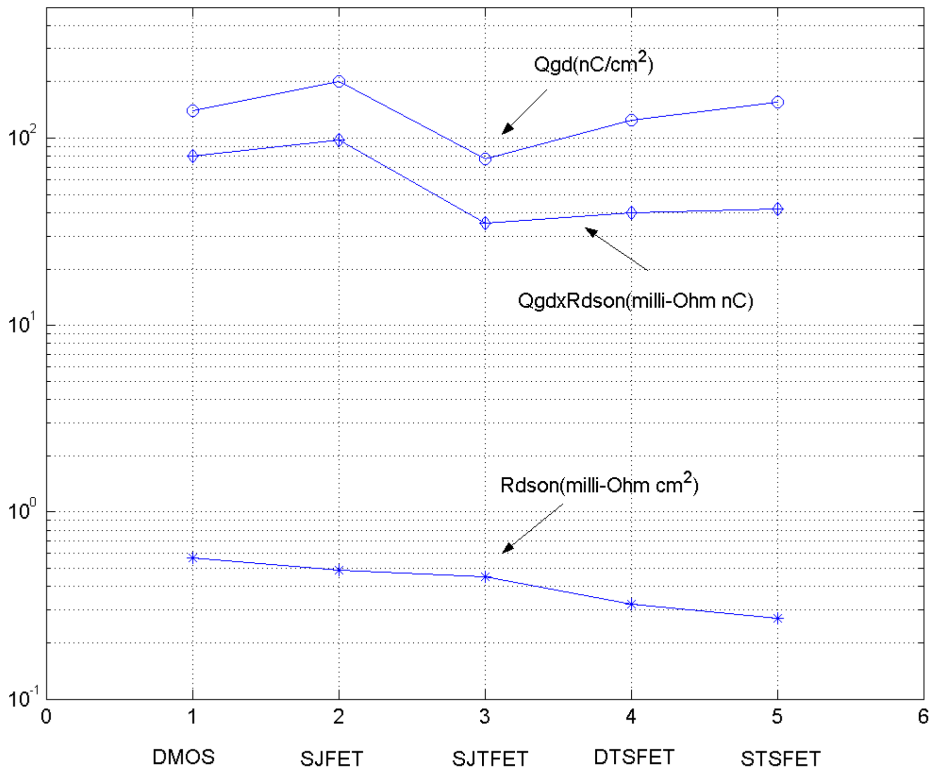

Figure 23 - Figures of Merit of 80-V SJFET and SFET Power Devices

Presented at the 7th International Seminar on Power Semiconductors, ISPS'06, Prague, Czech Republic, 2006.